DESIGN AND ANALYZE HIGH SPEED, POWER EFFICIENT FULL ADDER USING DIGITAL LOGIC TECHNIQUE

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Abstract— This paper proposed the design of high speed Full adder using digital logic technique. An adder is a digital circuit that performs addition of numbers. The adder is one of the most critical components of a processor. Adders are used not only in the arithmetic logic unit (ALU), but also in other parts of the processor. The Full adder is designed using transmission gate (TG) and Multiple Threshold CMOS (MTCMOS) technique on Tanner SPICE simulation. Performance estimation of design using latest logic techniques and their respective obtained parameter has given most efficient technique to implement Full adder for respective parameter.

Keyword— Full Adder, MTCMOS, TG.

I.   INTRODUCTION

The adder is one of the most critical components of a processor. Adder is used Arithmetic Logic Unit (ALU) and other component of processor. And it is increase demand for mobile electronic devices such as cellular phones and laptop computers. It is requires the use of power efficient VLSI circuits.

Full adder is the fundamental unit in circuits used for performing arithmetic operations i.e. multipliers, compressors and comparators. Therefore, It reducing power consumption of the full adders, It will reduce the overall power consumption of the whole system. The arithmetic operations are used as digital signal processing, image processing and microprocessors of the VLSI application.

1.1 Transmission Gate

Transmission gate is act as a simple switch circuit. Switch circuit is present a new class of logic circuits that used pass transistors or TG as a basic building block. As shown in Fig. I, the CMOS transmission gate consists of one PMOS and one NMOS transistor is connected in parallel. The gate voltages applied to these two transistors as complementary signals. The CMOS transmission gate operates as a bidirectional switch. The bidirectional switch is between the nodes A and B which is controlled by signal C. If the control signal C is equal to VDD, and then both transistors are turned on and it provide a low-resistance current path between the nodes A and B. The control signal C is low, and then both transistors will be off, and the path between the A and B will be open circuit. Fig. I. shows that the three other normally used symbolic representation of the transmission gate.[5]
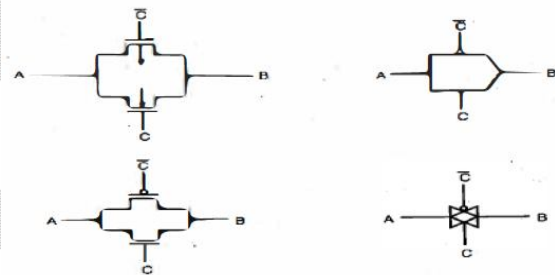

Fig 1 : Symbolic Representation of The Transmission Gate

1.2 MTCMOS Technique

Supply and threshold voltages are reduced with the scaling of CMOS technologies. The threshold voltage leads to an exponential increase in the subthreshold leakage current. In high performance integrated circuits (ICs), more than 40% of the total active mode energy can be dissipated due to the leakage currents. Leakage currents will be control the total energy consumption of the high performance ICs. The low leakage circuit technique is also known as multi threshold Voltage CMOS (MTCMOS).

The multi threshold CMOS technology has two main features. 1) "Active" and "sleep" operational nodes are associated with MTCMOS technology, for efficient power management. 2) Two different threshold voltages are used for N channel and P channel MOSFET in a single chip. This technique based on disconnecting the low threshold voltage (low-Vt) logic gates from the power supply and the ground line via cut-off high

threshold voltage (high-Vt) sleep transistors is also known as power gating. The schematic diagram of power gating technique using MTCMOS is shown in Fig. II. The transistors having low threshold voltage are used to implement the logic. The transistors having high threshold voltage are used to isolate the low threshold voltage
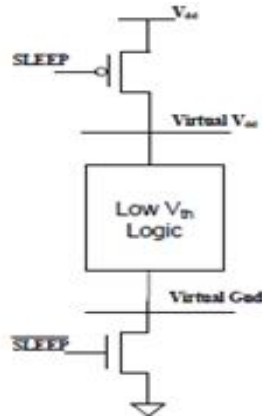

Fig. 2 : Power Gating Technique Using MTCMOS.

Transistors from supply voltage and ground during standby (sleep) mode to prevent leakage dissipation.

In the active mode, sleep transistors are turned on and the logic consisting of low Vt transistors can operate with high speed and low switching power dissipation. When the circuit is in sleep mode the high Vt transistors are turned off causing isolation of low Vt transistor from supply voltage and ground thereby reducing sub-threshold leakage current.

II. LITERATURE REVIEW

Krishnendu Dhar, Aanan Chatterjee, Sayan Chatterjee," *Design of an Energy Efficient, High Speed, Low Power Full Subtractor Using GDI Technique*"

In this paper proposed design of a full subtractor using Gate Diffusion Input (GDI) procedure which on simulation has been found to consume low power in conjunction with lesser delay time and fewer transistors while maintaining proper output-voltage swing. In order to establish the technology independence the present work has been performed in 150nm technology using Tanner SPICE and the layout has been concocted in Microwind. Comparisons with standard CMOS, transmission gate and CPL techniques showed a reduction of 72.00%, 63.16% and 58.82% in terms of transistor count, 99.68%, 88.78% and 99.99% in terms of average power consumption, 84.85%, 84.39% and 85.68% in terms of delay time and a significant 99.95%, 98.25 % and 99.99% in terms

of power delay product, respectively. Furthermore, a depreciation of 97.24%, 92.42% together with 95.10% in surface area is reaped when judged against a full subtractor composed adopting the popular CMOS approach, transmission gates and CPL, proportionately. Because of the noteworthy minimization of power delay product, transistor count and surface area the proposed logic can be useful in portable and low power applications [1].

Shyam Akashe, Nitesh Kumar Tiwari, Jayram Shrivas, Rajeev Sharma, "*A Novel High Speed & Power Efficient Half Adder Design Using MTCMOS Technique in 45 Nanometre Regime*"

In this paper proposed a MTCMOS technique that greatly reduces the power dissipation of the half adder. And also concluded that MTCMOS technique is better as compared to normal CMOS technique. MTCMOS is an effective circuit level technique that enhances the performance and provides low design methodologies by using both low and high threshold voltage transistors. From the simulation result it is cleared that after applying this technique we have reduced 56.55% in leakage current and 35.23% in leakage power[2].

Arkadiy Morgenshtei, Alexander Fish And Israel A. Wagner, "*Gate-Diffusion Input (Gdi) - A Technique For Low Power Design Of Digital Circuits: Analysis And Characterization*"

It has worked on GDI technique in which device under test was implemented in regular p-well CMOS processes, which casts a limitation on a GDI cell library. Still, even in limited-library based GDI circuits, significant improvements of performance are observed. Implementations of GDI circuits in SO1 or twin-well CMOS processes are expected to supply more power-delay efficient design, due to the use of a complete cell library with reduced transistor count. The advantages of GDI technique, namely Shannon-based design algorithm. 2-transistors implementation of complex logic functions and in-cell swing restoration under certain operating conditions are unique within existing low-power design techniques. This is together with positive measurement and simulation results provide evidence that GDI design might enrich the toolbox of VLSI circuit designers [3].

III. IMPLEMENTATION

3.1 Basic Full Adder
A full adder circuit is one of the basic building blocks of the digital design. The full adder operation can be stated as

follows: Given the three 1- bit inputs A, B, and Cin, it is to calculate Sum and Carry i.e [4][5].

Sum = (A xor B) xor Cin

Carry = A and B + Cin (A xor B)

The truth table of full adder is shown in Table I.

TABLE I : Truth Table of Full Adder

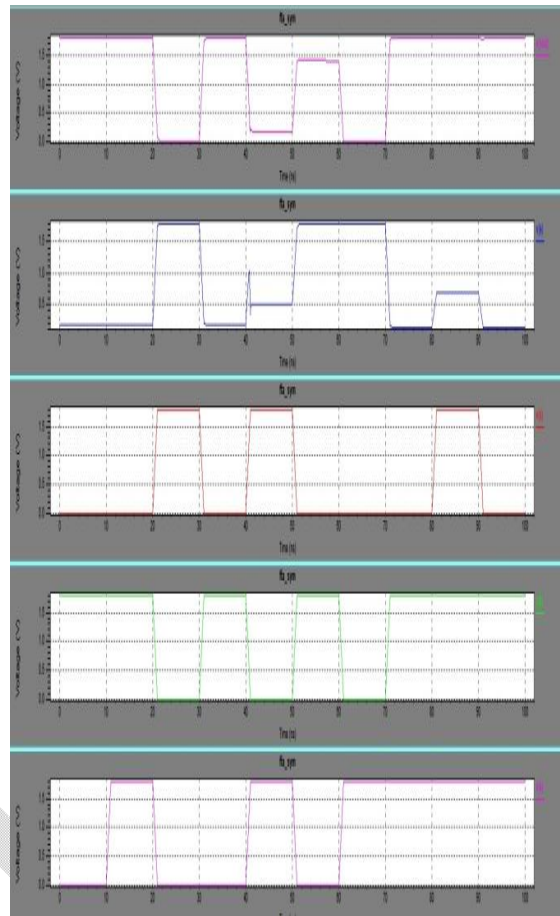| INPUT			OUTPUT	
CIN	A	B	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig 4 : Full adder Basked on Multiple Threshold CMOS Logic

3.2 Full Adder Based on Transmission Gate

The 20 transistors full adder has 20 numbers of transistors to perform the full adder function. The structure is given in the Fig 3 [6][7].
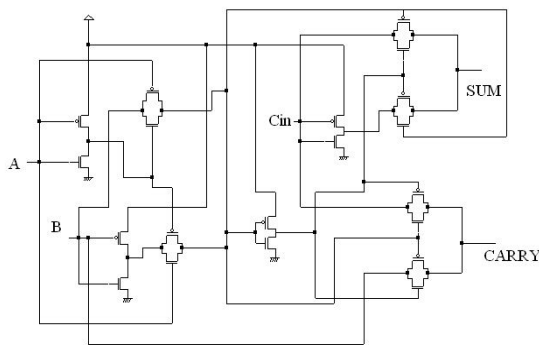
Fig 5. shows the circuit diagram of a one-bit full adder using the proposed technique in SOI CMOS technology [8].

Fig 3 : Structure of Full Adder using TG.

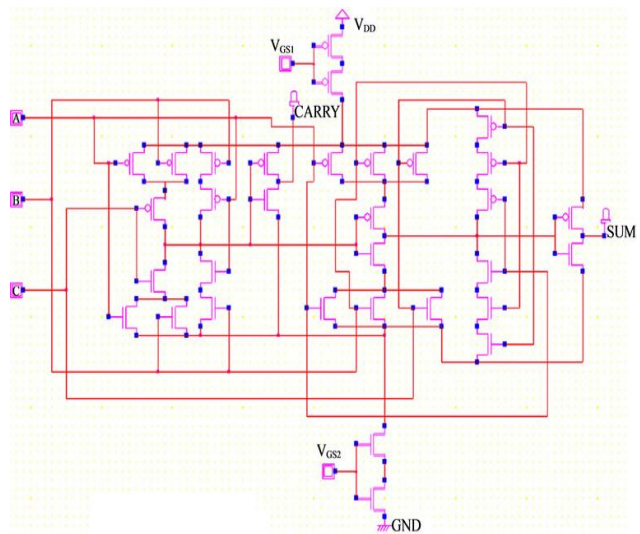Waveform of full Adder using transmission gate Fig 4.

Fig 5 : Structure of full adder using MTCMOS.

Waveform of full Adder using MTCMOS Fig .
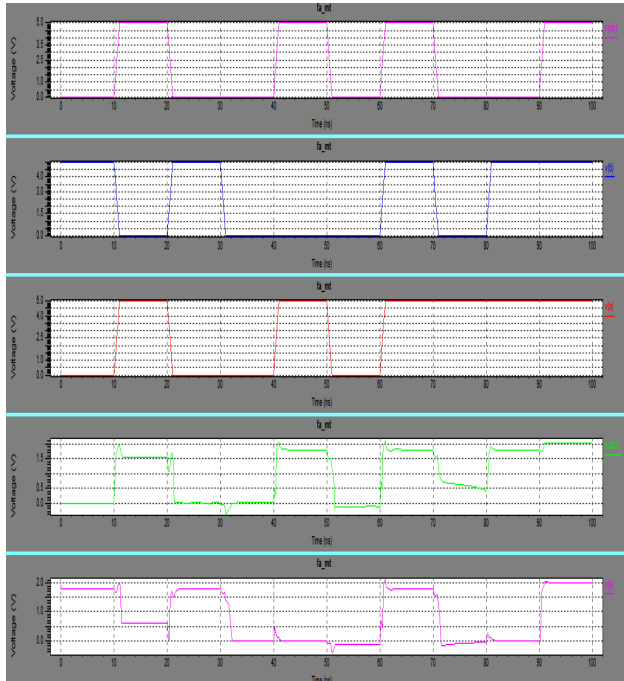

Fig 6 : Waveform of full Adder using MTCMOS.

IV.   COMPARISON AND RESULT

Table 2. Shows a comparative study of the performance parameter of the proposed full adder employing Transmission gate (TG) technique with respect to a full adder employing multiply threshold CMOS (MTCMOS) technique.

TABLE 2.Compertive Study of the Performance Parameter of Full Adder

Full adder		
	TG	MTCMOS
No. Of Transistor	20	34
Power dissipation	3.957 x 10-4 w	1.2611 x 10-5 w

V.   CONCULSION

The current work proposes the design of a full adder using transmission gate (TG) procedure which on simulation has been found to consume low power dissipation and fewer transistor. In order to establish the technology independence the present work has been performed in 180 nm technology using Tanner SPICE Simulation comparison with MTCMOS

shows reduction of 41.18% in terms of transistor count and 68.62% in terms of average power consumption respectively.

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